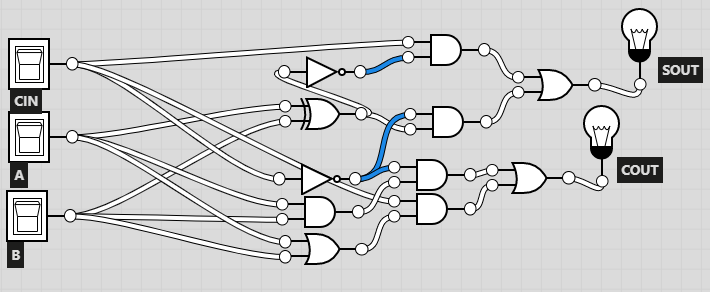
Gagan Gupta

05/05/19

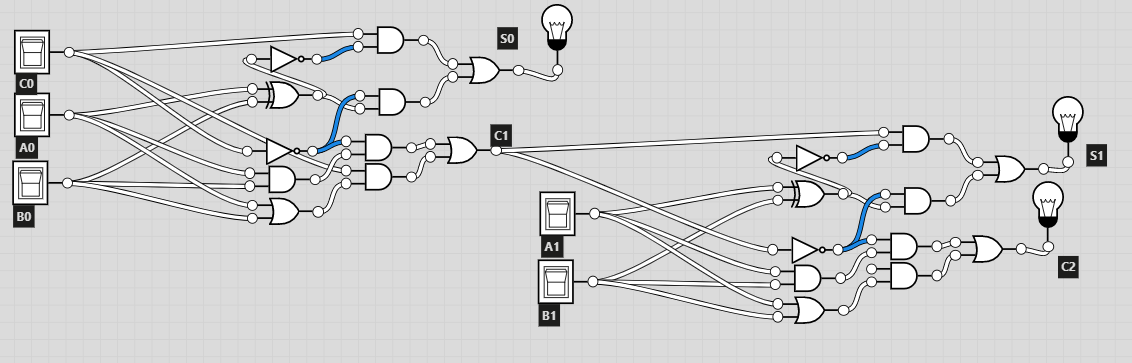
ELEN 21L F 2:15pm

Prelab#5

1. Write the algebraic logic expressions for the two outputs, SOUT and COUT, of a full adder in terms of the three inputs A, B, and CIN.
   1. SOUT = ((!CIN)\*(A^B))+((CIN)\*!(A^B))
   2. COUT = ((!CIN)\*(A\*B))+((CIN)\*(A+B))
2. Draw a logic gate schematic of a full adder.
   1. Clearly show the three inputs A, B, and CIN and the two outputs SOUT and COUT.
   2. Show all connections and internal connections and label all inputs and outputs.



1. Draw the schematic of a two-bit ripple carry adder that uses full adders.
   1. Define a symbol for your full adder. In the symbol, clearly label the inputs and outputs.
   2. You are doing a hierarchical design, so you will use two instances of the symbol for the full adder. (Do not redraw the internal circuitry for the full adder. Just use the symbol you have defined.) Clearly show the inputs of the 2-bit adder (A1, A0, B1, B0, and C0) and the outputs (S1, S0, and C2). Show all connections to the two-bit adder inputs and outputs. Show all internal connections for the two instances of the full adder components.



* 1. How many logic gates are on the path from the inputs A1, A0, B1, B0, and C0 to the output C2?
     1. 12

1. Using continuous assignment, write a Verilog module for a full adder. The module name should be myfulladd, and the inputs and outputs should be the same as in (1) above.

module myfulladd(CIN, A, B, SOUT, COUT);

input CIN, A, B;

output SOUT, COUT;

assign SOUT = ((~CIN)&(A^B))|((CIN)&~(A^B));

assign COUT = ((~CIN)&(A&B))|((CIN)&(A|B));

endmodule

1. Write a Verilog module for a two-bit ripple carry adder named myadder2 following the example of the four-bit adder in Figure 3.22 in the textbook. Use two instances of your myfulladd module from (4) above. Note that each instance should have a unique instance name as described on the page preceding Figure 3.22.

module myadder2(C0, A0, B0, A1, B1, S0, S1, C2);

input C0, A0, B0, A1, B1;

output S0, S1, C2;

wire C1;

myfulladd X1 (C0, A0, B0, S0, C1);

myfulladd X2 (C1, A1, B1, S1, C0);

endmodule